OTRA Based Piece-Wise Linear VTC Generators and Their Application in High-Frequency Sinusoid Generation

Sirish ORUGANTI, Yatin GILHOTRA, Neeta PANDEY, Rajeshwari PANDEY

Department of Electronics and Communication Engineering, Delhi Technological University, Main Bawana Road, Shahbad Daulatpur Village, Rohini, 110042 New Delhi, India

sirishoruganti@ieee.org, yatingilhotra999@gmail.com,neetapandey@dce.ac.in,rpandey@dce.ac.in

DOI: 10.15598/aeee.v15i5.2426

Abstract. *This paper proposes methods to generate various types of Linear Voltage Transfer Curves (VTC) using Operational Trans-Resistance Amplifier (OTRA) as the active block. It further goes on to propose methods to multiplex various individual Linear VTCs to obtain any form of Piece-Wise Linear Voltage Transfer Curves (PWL), which find many applications in the world of circuitry. One particular application has been highlighted, i.e. generation of High-Frequency Sinusoids. Simulations of the Circuits proposed via Cadence Virtuoso, using TowerJazz's 180 nm Technology Node have been reported, which satisfy the aim behind its development.*

Keywords

High-frequency, linear, OTRA, PWL, sinusoid, VTC.

1. Introduction

Voltage transfer curves are essential in any form of analog signal processing. They provide an appropriate output waveform based on the need. Wave shaping finds many uses in electronics, from voltage limitation, to signal processing, and waveform generation. Sinusoidal signals are an integral part of many electronic apparatus, from communication systems, to power conversion, control systems, data processing, and instruments [1] and [2].

The usual choice of active block for such implementations is the Operational Amplifier (Op-Amp). However, this comes with many disadvantages. Op-Amp based circuits are limited by their low slew rate, and low bandwidth of operation, which makes them undesirable for high-frequency and high-speed operations. Current-mode processing is a leading choice of today's engineers, which gives us many advantages like high slew rate. As such, it is more linear, more dynamic, and faster in operation as detailed in [3]. This has made current-mode active blocks increasingly popular. The OTRA block used in this work offers a much higher pole (corner frequency) than the generic Op-Amp, and a higher bandwidth of operation. Many applications of the OTRA have emerged in recent times, which indicate the usefulness of OTRA [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19] and [20].

Several PWL VTC and sinusoidal oscillators using current-mode active blocks exist in literature. Current Limiters based on the active block CDTA, and their practicality are detailed in [21]. Methods to synthesise PWL VTCs have been discussed in [22], which can be modified for our use. CDTA [23] and [24], and OTRA [25], [26] and [27] based oscillators show the application of current-mode active blocks in generation of sinusoids. However, they use harmonic methods, which usually fail in high frequencies. Also, the solution in [24] has current inputs, making it impractical. None of the cited works use current-mode active blocks in PWL VTC generation to produce a sinusoid, which shows the gap in research, and the motivation behind this work.

In this work, we propose methods to generate any desired PWL VTC using OTRA active block, which gives us benefits of current-mode processing [3]. One specific use case of voltage controlled high-frequency sinusoid generation is detailed, where voltage-mode active blocks and harmonic methods fail. All the circuits proposed have been simulated successfully, and the results are included.

2. The OTRA

The Operational Trans-Resistance Amplifier (OTRA) is a three-terminal device as shown in Fig. 1.

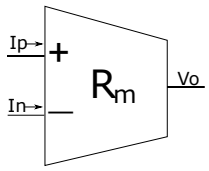


Fig. 1: OTRA block diagram.

The OTRA amplifies the difference of the currents I_p and I_n and the output is the voltage V_o in accordance to port characteristics as expressed by Eq. (1). The R_m is known as the trans-resistance gain, and its value approaches infinity for an ideal OTRA, which in turn forces the input currents to be equal. For ideal operation, V_p and V_n should be zero. Also, V_o should not depend on the current drawn from the output terminal, i.e. I_o.

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \cdot \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix}. \tag{1}$$

The output of an ideal OTRA reaches positive or negative saturation levels (V_{DD} or V_{SS}) if used in an open loop configuration as the R_m is infinite. Thus, for linear applications the OTRA must be used in a negative feedback configuration. The OTRA used in this work [28] is shown in Fig. 2. The values of transistor W/L ratios, V_{B1} and I_B may be referenced from [28]. The OTRA gives us a Gain-Bandwidth Product of 600 GHz Ω, which makes it suitable for High-Frequency Applications.

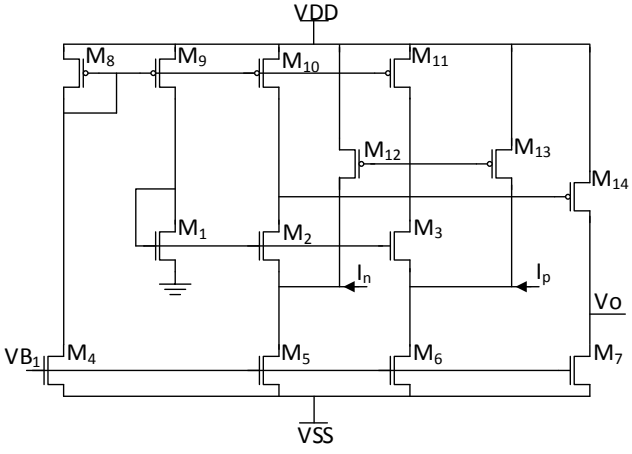


Fig. 2: OTRA CMOS circuit [14].

3. Proposed VTC Generators

Positive and negative slope VTC generators based on OTRA are proposed in this section.

The schematic of the positive generator is shown in Fig. 3, where the OTRA is used in the non-inverting amplifier configuration [28]. The output voltage V_{out} is related to the input voltage V_{in} by Eq. (2).

$$V_{out} = \frac{R_f}{R_{in}} V_{in} + \frac{R_f}{R_b} V_{bias}. \tag{2}$$

The first term in the RHS of Eq. (2) provides the desired slope, and the second term introduces the required DC offset.

Figure 4 depicts the negative slope VTC generator. Here, the OTRA is used in inverting amplifier configuration [29]. The output voltage V_{out} is related to the input voltage V_{in} by Eq. (3).

$$V_{out} = -\frac{R_f}{R_{in}} V_{in} + \frac{R_f}{R_b} V_{bias}. \tag{3}$$

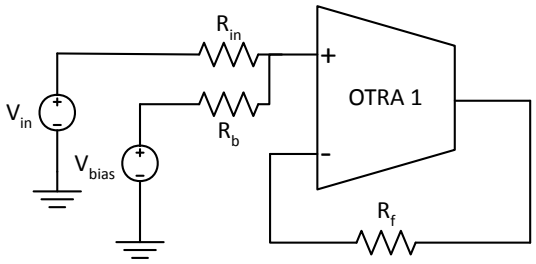


Fig. 3: Schematic for positive slope linear VTC generator.

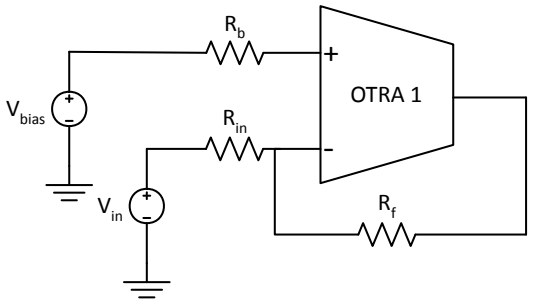


Fig. 4: Schematic for negative slope linear VTC generator.

4. Proposed PWL VTC Generators

The individual VTC generators as proposed in Sec. 3. can be multiplexed to generate a complex piece-wise linear voltage transfer curve (PWL VTC). To switch

$$\tau_{TG} = \frac{C_L}{2}\left[\frac{1}{K_p\left(|V_{DD}+V_X|-|V_{Tp}|\right)^2}\left\{-V_{SS}-\frac{K_n\left((V_X-V_{Tn})^3-(V_X-V_{Tn}-V_{SS})^3\right)}{3K_p\left(V_{DD}-V_X-V_{Tp}\right)^2}\right\}+\right.$$
$$\left.+\frac{1}{K_n(V_X-V_{SS}-V_{Tn})^2}\left\{-V_{DD}-\frac{K_p\left((V_x-|V_{Tp}|)^3-(|V_{DD}+V_X|-V_{Tp})^3\right)}{3K_n\left(V_X-V_{SS}-V_{Tn}\right)^2}\right\}\right]. \quad (4)$$

between appropriate VTCs at breakpoints, comparators need to be used, which compare the input voltage with the breakpoint voltage. The comparators feed a digital logic circuit, which needs to be synthesised for each use case. The logic gates will operate between V_{DD} and V_{SS}. The digital logic should be designed such that one and exactly one channel of the multiplexer is active for each and every piece of the PWL VTC, i.e. for all values of input voltage, exactly one of (S0, S0'), (S1, S1'), or (S2, S2') are active, and the rest inactive.

The digital logic controls the output of the analog multiplexer formed by transmission. The multiplexer lets the output from the desired VTC Generator pass based on the digital control logic. Standard CMOS design techniques may be used to design the gates [30].

Figure 5 and Fig. 6 show the implementation of the analog multiplexer and the OTRA based comparator respectively.

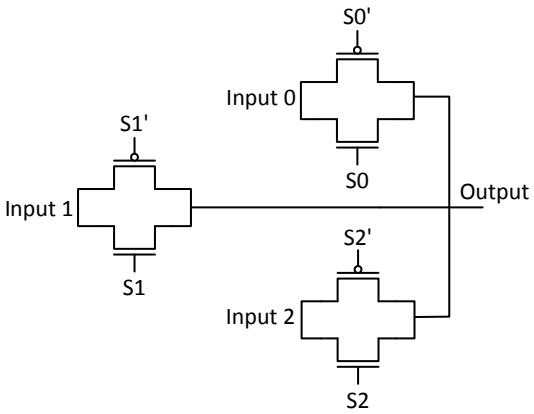


Fig. 5: Analog multiplexer made with transmission gates.

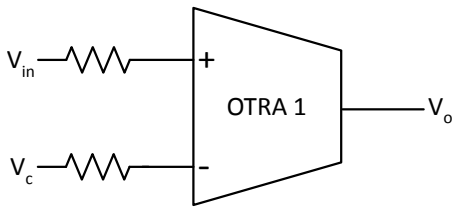


Fig. 6: OTRA working as a comparator in open-loop configuration.

Using the blocks of Fig. 3, Fig. 4, Fig. 5 and Fig. 6, and the procedure outlined above, any desired PWL VTC can be generated. A simple use case of this has been illustrated in Sec. 5. , which uses a PWL VTC to convert a triangular wave into a sinusoid.

5. Application: High-Frequency Sinusoid Generation

A triangular wave, when passed through an appropriate PWL VTC, can produce an approximate sinusoid, as detailed in [1]. This concept has been used to illustrate the usefulness of the PWL VTC generators proposed in this work.

The triangular wave is generated from a voltage-controlled ring oscillator (demarcated by dashed line in Fig. 7) as detailed in [30], with transmission gates to control the delays, connected to an integrator circuit based on OTRA [29]. Figure 7 shows the triangular wave generator used. All the transistors in the Voltage Controlled Ring Oscillator have the W/L ratio as 1 µ/0.5 µ.

Assuming the tripping voltage for an inverter is $(V_{DD}+V_{ss})/2$, we get the equation for the propagation delay through the transmission gate as detailed in Eq. (4). Where the C_L is the input capacitance of inverter, and V_X the DC control voltage. Equation (5) gives the delay for one inverter, as explained in [30].

$$\tau_{inv} = \frac{\tau_{phl}+\tau_{plh}}{2}. \quad (5)$$

Thus, the frequency of the oscillator can be given by Eq. (6).

$$f = \frac{1}{10(\tau_{TG}+\tau_{inv})}. \quad (6)$$

OTRA 1 is a comparator which compares this rectangular wave to ground, and outputs a sharper rectangular wave.

OTRA 2 is a lossy integrator [29]. It integrates the rectangular wave into a triangular wave. OTRA 3 is used to boost the output of OTRA 2 to a rail to rail

value. This outputs a triangular wave, which is passed on to the PWL VTC generator to output a sinusoid.

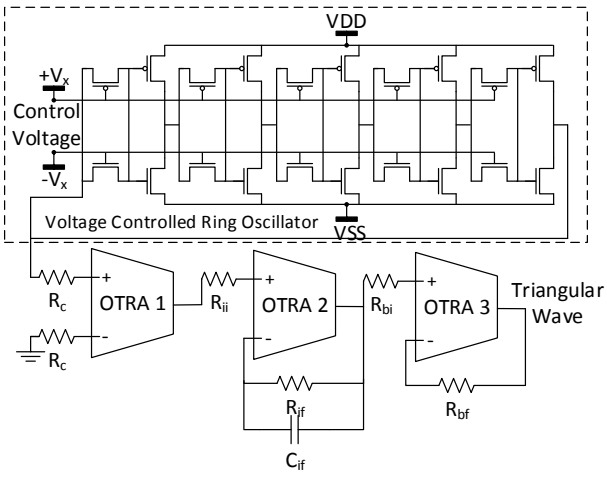


Fig. 7: Triangular wave generator.

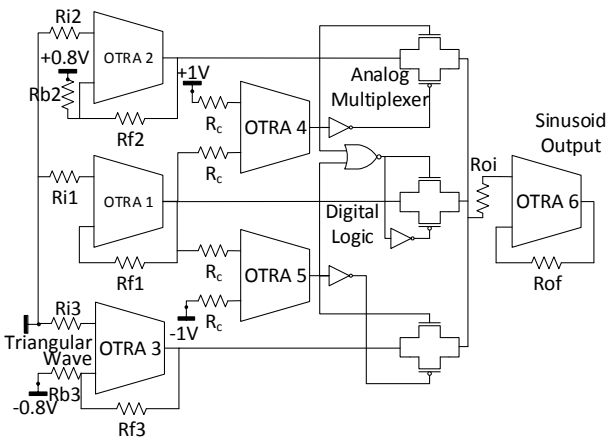


Fig. 8: PWL VTC generator for triangular to sinusoid conversion.

The PWL VTC generator for triangular to sinusoidal conversion is as shown in Fig. 8 OTRAs 1, 2 and 3 are used to generate the individual PWLs as follows:

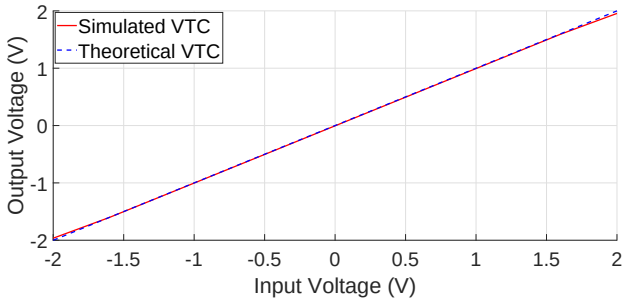
- OTRA 1 generates a VTC with slope = -1 and $V_{bias} = 0$ V.
- OTRA 2 generates a VTC with slope = -0.4 and $V_{bias} = +0.6$ V.
- OTRA 3 generates a VTC with slope = -0.4 and $V_{bias} = -0.6$ V.

OTRAs 4 and 5 are connected as comparators with reference voltages $+1$ V and -1 V respectively.

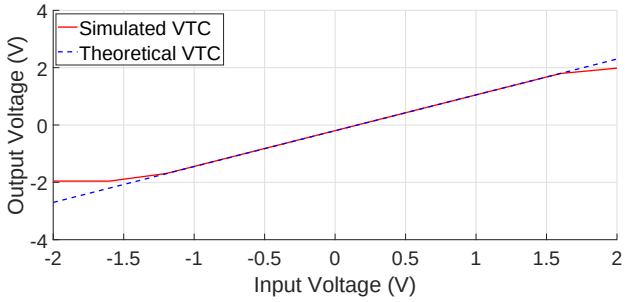
OTRA 6 is the output stage that converts the PWL VTC output to a rail to rail sinusoid. The output of an OTRA based amplifier near the rails is naturally slewed, and this can be used to our advantage to obtain a curvature in the transient waveform near the rails.

6. Simulation Results

The functional verification of proposed circuits is carried out on Cadence Virtuoso ADE using TowerJazz's 180 nm technology node. V_{DD} is taken as $+2$ V and V_{SS} is taken to be -2 V globally for simulations.

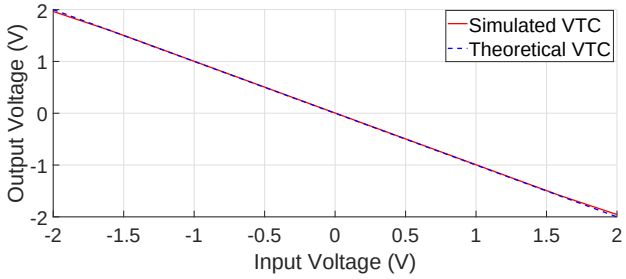


(a) Positive VTC without bias.

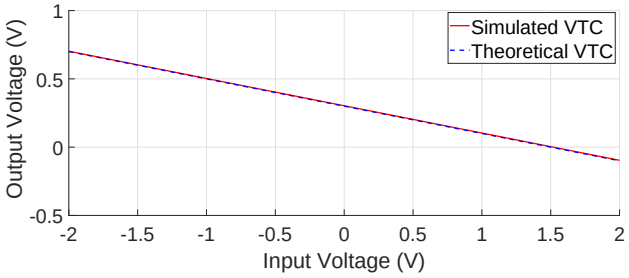


(b) Positive VTC with bias.

Fig. 9: Positive VTC.



(a) Negative VTC without Bias.



(b) Negative VTC with bias.

Fig. 10: Negative VTC.

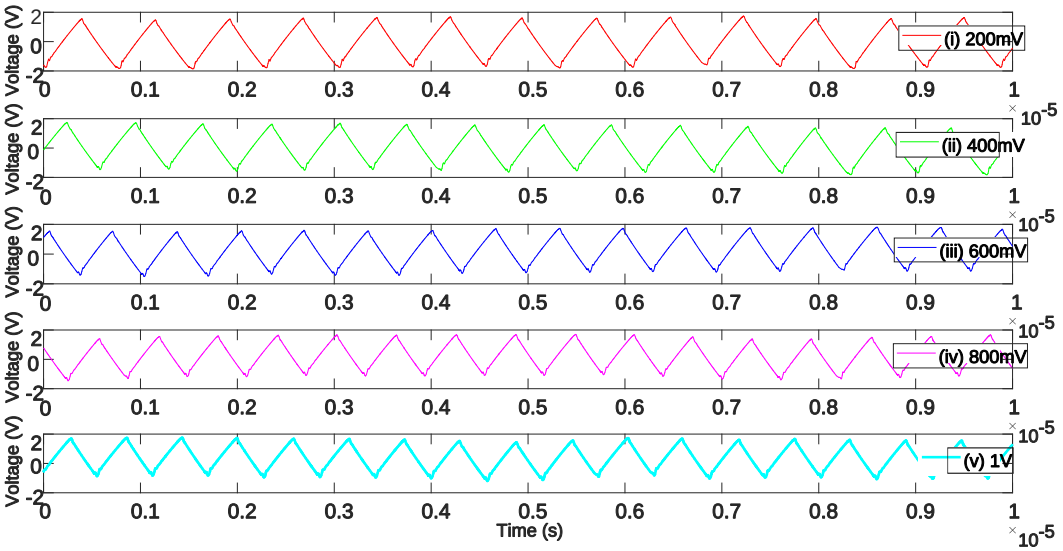


Fig. 11: Frequency variation of triangular wave output for V_{bias} values as (i) 200 mV, (ii) 400 mV, (iii) 600 mV, (iv) 800 mV and (v) 1 V.

The simulated and theoretical output of the positive VTC generator without and with bias have been reported in Fig. 9(a) and Fig. 9(b) respectively. Similar outputs for negative VTC generators are placed in Fig. 10(a) and Fig. 10(b). For these simulations, the values of R_b and R_{in} were taken to be 10 $k\Omega$, V_{bias} and R_f were varied accordingly.

The operation of the proposed VTC generators is tested against process corner variations, for typical, fast-fast, fast-slow, slow-fast and slow-slow corners. Simulation results are shown in Fig. 12, which prove that the outputs are insensitive to process variations.

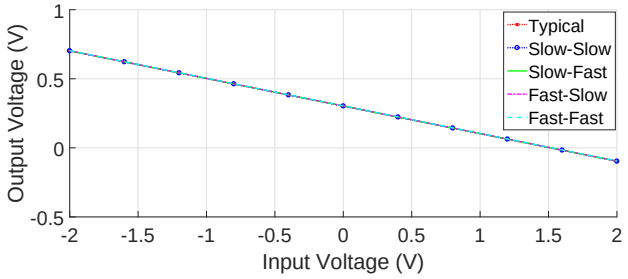


Fig. 12: Process corner variation.

Further, to test the effect of temperature variations, simulations were carried out by varying the temperature of the simulation environment, from −20 °C to +60 °C, in steps of 20 °C. The simulated output is shown in Fig. 13. The plot shows that the circuits are resilient to any forms of temperature variations.

Transient response of the triangular wave generator is shown in Fig. 11, which also shows variation in frequency with respect to control voltage V_X.

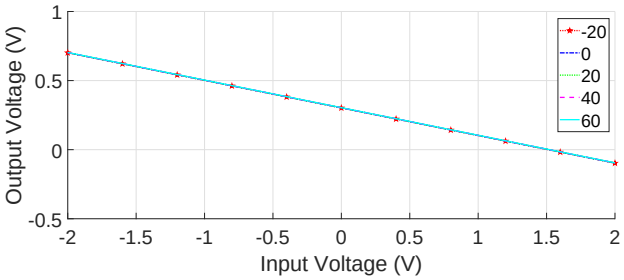


Fig. 13: Temperature variation.

To verify the functionality of the sinusoid generator, the different VTCs chosen are as follows:

- OTRA 1 is generating a VTC with slope = −1 and V_{bias} = 0 V. The values of R_{i1} and R_{f1} are both taken to be 100 KΩ.
- OTRA 2 is generating a VTC with slope = −0.4 and V_{bias} = +0.6 V. The values of R_{i2} and R_{f2} are taken to be 100 KΩ and 40 KΩ respectively.
- OTRA 3 is generating a VTC with slope = −0.4 and V_{bias} = −0.6 V. The values of R_{i3} and R_{f3} are taken to be 100 KΩ and 40 KΩ respectively.

R_c was taken to be 10 KΩ, and standard CMOS logic gates were used for the digital logic, as detailed in [30].

Theoretically, by Eq. (6), the frequency for the VCO at V_X = 180 mV was found to be 1.13 MHz. On simulation, we found it was equal to 1 MHz. It can thus be calculated that the frequency deviation between theoretical and experimental frequencies is 13 % for the case implemented. The experimental value for frequency is lower than theoretical as the theory does not account

for delays caused by the parasitic resistances and capacitances, which increase the time, and thus reduce the frequency.

The three individual VTCs are shown in Fig. 14, and the transient response output of the PWL VTC Generator is shown in Fig. 15.

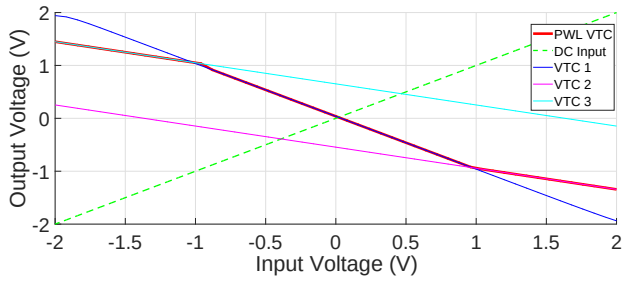


Fig. 14: The individual VTCs and combined PWL VTC.

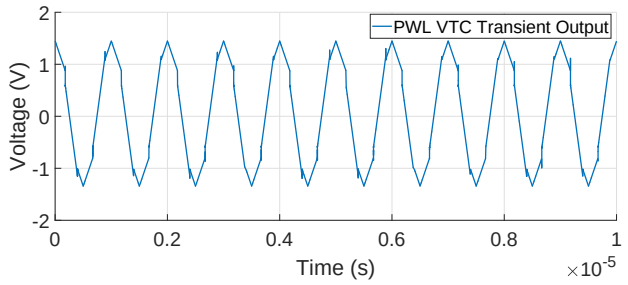


Fig. 15: Transient response of the PWL VTC generator.

In the output stage, R_{oi} and R_{of} were taken to be 10 KΩ and 25 KΩ respectively. The transient output of the output stage is shown in Fig. 16, in comparison with a standard sine wave. The obtained waveform slightly deviates from the ideal waveform, as we have used only three VTC sections. However, on increasing the number of VTC sections, this deviation can be reduced.

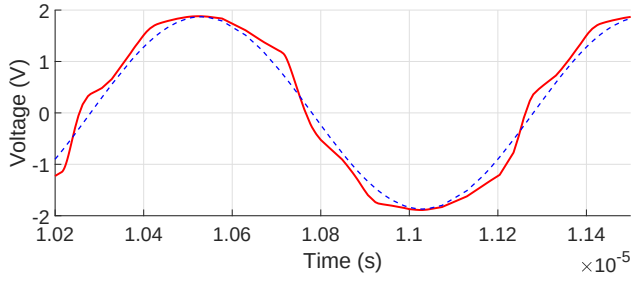


Fig. 16: Transient response of the output stage.

Figure 17 shows the frequency spectrum of the output in comparison with that of an actual sine wave for 1 MHz frequency. As can be clearly observed, there is a good level of accuracy achieved in delivering a sinusoid output. Total Harmonic Distortion was calculated for the generated sinusoid, up to five harmonics, and the value was found to be 9.3776 %. The THD can be further improved by increasing the number of VTC sections.

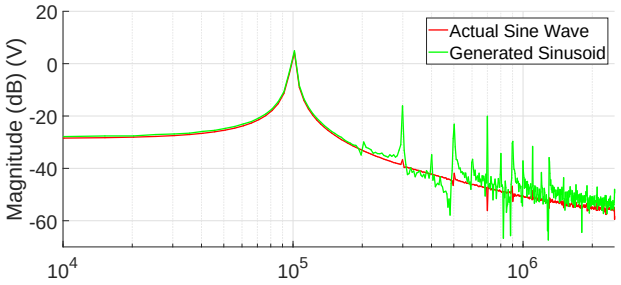


Fig. 17: Frequency spectrum of the sinusoid generated.

Monte-Carlo Analysis was done to test the performance of the circuit against component value variations. The resistors were varied with 10 % tolerance from the nominal value. The test was performed for 500 samples. It was found that for a < 5 % mismatch with respect to the nominal waveform, over 83 % of the samples passed the Monte-Carlo Simulation, which illustrates the low sensitivity to passive component parameter variations that our circuit exhibits. Monte-Carlo Analysis was also performed on the MOSFET Width parameter (W) with 5 % tolerance, < 5 % mismatch pass mark, and 500 samples yielded a pass for over 70 % of the samples. As on changing the W, the frequency of the VCO changes, the waveform is not a match to the nominal value, and shows variation. Also, the OTRA Gain is also changed, thus causing the mismatch.

Analyses for testing the behavior of the circuit against parasitic elements were performed. The input capacitance for the Inverter was 83 fF, and for the NOR Gate was 104 fF. The Output Capacitance of the OTRA was found to be 3.04 pF, which is much larger than that of the Digital Logic, and hence, the OTRA will dominate in the parasitic effects. It can be noted from [28] that for the low gain case as used in this work, the OTRA will function well for frequencies much higher than the ones at which we are generating the sinusoid. Hence, the effect of parasitics is negligible in our work.

7. Conclusion

In this work, positive and negative slope linear VTC generators using OTRA have been proposed, which can be designed to generate any linear curve as per the design rules mentioned in Eq. (2) and Eq. (3). They can be multiplexed to generate any desired PWL VTC as detailed in Sec. 4. As a particular application,

three different VTCs have been multiplexed to generate a PWL VTC that converts a triangular wave into a sinusoid. This is useful in generating high-frequency sinusoids where harmonic oscillator methods and other voltage mode active block based circuits fail.

Simulation results on Cadence Virtuoso using TowerJazz's 180 nm technology node have been reported for all the circuits proposed. The VTC generators were tested for process corner and temperature variations, and were found to be extremely resilient to their changes. The frequency spectrum of the generated sinusoid is found to be very close to that of an original sine wave.

Acknowledgment

The authors wish to thank Mr. Nitish, Graduate Student, Dept. of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, USA, and Mr. T. R. Aashish, Research Scholar, Department of Electrical Engineering, Indian Institute of Technology, Delhi, for their support during simulations.

References

[1] SEDRA, A. S. and K. C. SMITH. *Microelectronic Circuits*. 7th ed. New York: Oxford University Press, 2015. ISBN 978–0–19–933913–6.

[2] RAZAVI, B. *Fundamentals of Microelectronics*. 2nd ed. Hoboken: John Wiley & Sons, 2014. ISBN 978-1-118-15632-2.

[3] YUAN, F. *CMOS Current-Mode Circuits for Data Communications*. 1st ed. Hoboken: Springer, 2007. ISBN 978-1-4419-3999-9.

[4] ORUGANTI, S., N. PANDEY and R. PANDEY. OTRA Based First-Order Universal Filter. In: *International Conference on Advanced Research and Innovation (ICARI)*. New Delhi: Delhi Technical Campus, 2017.

[5] ANURAG, R., N. PANDEY, R. PANDEY and R. VIJAY. OTRA Based Precision Rectifier. *i-manager's Journal on Electronics Engineering (JELE)*. 2015, vol. 6, iss. 1, pp. 21–27. ISSN 2229-7286.

[6] BOTHRA, M., R. PANDEY, N. PANDEY and S. K. PAUL. Operational Trans-Resistance Amplifier Based Tunable Wave Active Filter. *Radioengineering*. 2013, vol. 22, iss. 1, pp. 159–166. ISSN 1210-2512.

[7] SALAMA, K. N. and A. M. SOLIMAN. Universal filters using operational Transresistance amplifiers. *AEU-Archiv fur Elektronik und Ubertragungstechnik*. 1999, vol. 53, iss. 1, pp. 49–52. ISSN 0001-1096.

[8] AKIR, C. C., U. CAM and O. CICEKOGLU. Novel all pass filter configuration employing single OTRA. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2005, vol. 52, iss. 3, pp. 122–125. ISSN 1558-3791. DOI: 10.1109/TCSII.2004.842055.

[9] KILINC, A. and U. CAM. Transimpedance Type Fully Integrated Biquadratic Filters Using Operational Transresistance Amplifiers. *Analog Integrated Circuits and Signal Processing*. 2006, vol. 47, iss. 2, pp. 193–198. ISSN 1573-1979. DOI: 10.1007/s10470-006-2963-0.

[10] KILINC, A., A. U. KESKIN and U. CAM. Voltage-mode Multifunction Biquads employing a single Operational Transresistance Amplifier. In: *IEEE 15th Signal Processing and Communications Applications (SIU)*. Eskisehir: IEEE, 2007, pp. 1–4. ISBN 1-4244-0719-2. DOI: 10.1109/SIU.2007.4298823.

[11] CAM, U. U., F. KACAR, O. CICEKOGLU, H. KUNTMAN and A. KUNTMAN. Novel Grounded Parallel Immittance Simulator Topologies Employing Single OTRA. *AEU-International Journal of Electronics and Communications*. 2003, vol. 57, no. 4, pp. 287–290. ISSN 1434-8411. DOI: 10.1078/1434-8411-54100173.

[12] CAM, U. U., F. KACAR, O. CICEKOGLU, H. KUNTMAN and A. KUNTMAN. Novel Two OTRA-Based Grounded Immitance Simulator Topologies. *Analog Integrated Circuits and Signal Processing*. 2004, vol. 39, no. 2, pp. 169–175. ISSN 1573-1979. DOI: 10.1023/B:ALOG.0000024064.73784.58.

[13] PANDEY, R., N. PANDEY, S. K. PAUL, A. SINGH, B. SRIRAM and K. TRIVEDI. Novel grounded inductance simulator using single OTRA. *International Journal of Circuit Theory and Applications*. 2014, vol. 42, no. 10, pp. 1069–1079. ISSN 1097-007X. DOI: 10.1002/cta.1905.

[14] SALAMA, K. N. and A. M. SOLIMAN. Novel oscillators using operational transresistance amplifier. *Microelectronics Journal*. 2000, vol. 31, iss. 1, pp. 39–47. ISSN 0026-2692. DOI: 10.1016/S0026-2692(99)00087-7.

[15] CAM, U. A novel single-resistance-controlled sinusoidal oscillator employing single operational transresistance amplifier. *Analog Integrated Circuits and Signal Processing*. 2000,

vol. 32, iss. 2, pp. 183–186. ISSN 1573-1979. DOI: 10.1023/A:1019586328253.

[16] HOU, C.-L., H.-C. CHIEN and Y.-K. LO. Square-wave generators employing OTRAs View Document. *IEE Proceedings - Circuits, Devices and Systems*. 2005, vol. 152, iss. 6, pp. 718–722. ISSN 1350-2409. DOI: 10.1049/ip-cds:20045167.

[17] LO, Y.-K. and H.-C. CHIEN. Current-Mode monostable multivibrators using OTRAs. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2006, vol. 53, iss. 11, pp. 1274–1278. ISSN 1558-3791. DOI: 10.1109/TCSII.2006.882361.

[18] LO, Y.-K. and H.-C. CHIEN. Switch-Controllable OTRA-Based Square/Triangular Waveform Generator. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2007, vol. 54, iss. 12, pp. 1110–1114. ISSN 1558-3791. DOI: 10.1109/TCSII.2007.905879.

[19] LO, Y.-K. and H.-C. CHIEN. Single OTRA-based current-mode monostable multivibrator with two triggering modes and a reduced recovery time. *IET Circuits, Devices & Systems*. 2007, vol. 1, iss. 3, pp. 257–261. ISSN 1751-8598. DOI: 10.1049/iet-cds:20060359.

[20] LO, Y.-K., H.-C. CHIEN and H.-J. CHIU. Switch-controllable OTRA-based bistable multivibrators. *IET Circuits, Devices & Systems*. 2008, vol. 2, iss. 4, pp. 373–382. ISSN 1751-8598. DOI: 10.1049/iet-cds:20080011.

[21] PUKKALANUN, T. and W. TANGSRIRAT. CDTA-Based Current Limiters and Applications. In: *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. Macao: IEEE, 2007, pp. 1070–1073. ISBN 978-1-4244-2342-2. DOI: 10.1109/APCCAS.2008.4746209.

[22] SCANLAN, S. O. Synthesis of Piecewise-Linear Chaotic Oscillators with Prescribed Eigenvalues. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*. 2001, vol. 48, iss. 9, pp. 1057–1064. ISSN 1057-7122. DOI: 10.1109/81.948433.

[23] PISITCHALERMPONG, S., W. TANGSRIRAT and W. SURAKAMPONTORN. CDBA-based Multiphase Sinusoidal Oscillator Using Grounded Capacitors. In: *International Joint Conference SICE-ICASE*. Busan: IEEE, 2007, pp. 5762–5765. ISBN 89-950038-4-7. DOI: 10.1109/SICE.2006.314650.

[24] PRASERTSOM, D. and W. TANGSRIRAT. CDBA-Based Sinusoidal Quadrature Oscillator with Current Controlled Amplitude. In: *10th International Symposium on Communications and Information Technologies (ISCIT)*. Tokyo: IEEE, 2010, pp. 187–191. ISBN 978-1-4244-7009-9. DOI: 10.1109/ISCIT.2010.5664835.

[25] PANDEY, R., N. PANDEY, M. BOTHRA and S. K. PAUL. Operational Transresistance Amplifier-Based Multiphase Sinusoidal Oscillators. *Journal of Electrical and Computer Engineering*. 2011, vol. 2011, iss. 1, pp. 1–8. ISSN 2088-8708. DOI: 10.1155/2011/586853.

[26] PANDEY, R., N. PANDEY, R. KUMAR and G. SOLANKI. A novel OTRA based oscillator with non-interactive control. In: *2010 International Conference on Computer and Communication Technology (ICCCT)*. Allahabad: IEEE, 2010, pp. 658–660. ISBN 978-1-4244-9033-2. DOI: 10.1109/ICCCT.2010.5640448.

[27] PANDEY, R., N. PANDEY and S. K. PAUL. MOS-C Third Order Quadrature Oscillator Using OTRA. In: *2012 Third International Conference on Computer and Communication Technology (ICCCT)*. Allahabad: IEEE, 2013, pp. 77–80. ISBN 978-1-4673-3149-4. DOI: 10.1109/ICCCT.2012.24.

[28] MOSTAFA, H. and A. M. SOLIMAN. A Modified CMOS Realization of the Operational Transresistance Amplifier (OTRA). *Frequenz*. 2006, vol. 60, iss. 3–4, pp. 70–76. ISSN 2191-6349. DOI: 10.1515/FREQ.2006.60.3-4.70.

[29] SALAMA, K. N. and A. M. SOLIMAN. CMOS operational transresistance amplifier for analog signal processing). *Microelectronics Journal*. 1999, vol. 30, iss. 3, pp. 235–245. ISSN 0026-2692. DOI: 10.1016/S0026-2692(98)00112-8.

[30] RABAEY, J. M. *Digital Integrated Circuits: A Design Perspective*. 1st ed. Saddle River: Prentice Hall, 1996. ISBN 978-0-131-78609-7.

About Authors

Sirish ORUGANTI was born in Visakhapatnam, Andhra Pradesh, India. He is currently an undergraduate student, pursuing his Bachelor of Technology in Electronics and Communication Engineering from Delhi Technological University. His research interests include Analog and Mixed-Signal VLSI Design and Low-Power VLSI Design.

Yatin GILHOTRA was born in Ambala, Haryana, India. He is currently an undergraduate student,

pursuing his Bachelor of Technology in Electronics and Communication Engineering from Delhi Technological University. His research interests include Low-Power VLSI Design, Mixed-Signal VLSI Design, Analog Design, Neural Detectors and Brain Machine Interfaces.

Neeta PANDEY is currently a Professor in Department of Electronics and Communication Engineering, Delhi Technological University. She did her M.E. in Microelectronics from Birla Institute of Technology and Sciences, Pilani and Ph.D. from Guru Gobind Singh Indraprastha University Delhi. She is a life member of ISTE, and Senior Member of IEEE, USA. Her research interests are in Analog and Digital VLSI Design.

Rajeshwari PANDEY is currently a Professor in Department of Electronics and Communication Engineering, Delhi Technological University. She did her M.E in Electronics and Control from BITS, Pilani, Rajasthan, India and Ph.D. from Faculty of Technology, Delhi University, India. She is a life member of IETE, ISTE and member of IEEE, and IEEE WIE for over 12 years. Her research interests include Analog Integrated Circuits, and Microelectronics.